03947-P0010A WWW/HJP

UNITED STATES PATENT APPLICATION

of

Ku Rak Jung
Usan Apt. 107-1404, Munheung-dong 787-1
Buk-gu
Gwangju si, Korea

Jun Hee Kang
Dongsung 204-210, Saetbyeolmaeul
Bundang-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, Korea

Alex F. Kirichenko
175 Clearbrook Road
Elmsford, NY 10523

and

Saad Sarwana
175 Clearbrook Road
Elmsford, NY 10523

for

ARITHMETIC AND LOGIC UNIT USING HALF ADDER

Attorneys for Applicants
Wesley W. Whitmyer, Jr., Registration No. 33,558
Hyun Jong Park, Limited Recognition
ST.ONGE STEWARD JOHNSTON & REENS LLC
986 Bedford Street
Stamford, CT 06905-5619
203 324-6155

Express Mail No. EL 889 892 921 US

ARITHMETIC AND LOGIC UNIT USING HALF ADDER

[0001] This application claims priority of pending Korean Patent Application 2004-26148 filed April 16, 2004.

Field of the Invention

[0002] The present invention relates to an arithmetic and logic unit (ALU), and more particularly, to a high-performance ALU that can be operated as an OR gate, an AND gate, an adder gate and an exclusive OR gate using a superconductor rapid single flux quantum logic device as a half adder.

Background of the Related Art

[0003] Development of information communication technology increasingly requires improved performances of computers and microprocessors used for the technical fields.

[0004] The performances of computers and microprocessors are determined by the performance of a central processing unit (CPU). Especially, the performance of an ALU constructing the CPU is very important.

[0005] FIG. 1 shows a structure of an ALU generally used. As shown in FIG. 1, the ALU is composed of a combination of semiconductor logic circuits including an exclusive OR gate 11, an AND gate 12, an OR gate 13, a full adder 14 and a multiplexer 15. The logic circuits determine digital output values based on to voltage states.

[0006] However, the ALU including the semiconductor logic circuits has a relatively low operating speed. To significantly improve the performance of the ALU, it is more preferable to determine a digital value using a voltage pulse than to determine the digital value according to a voltage state.

[0007] There has been proposed a superconductor rapid single flux quantum logic device as a logic circuit that determines a digital value using a voltage pulse. A half adder or a T flip-flop using the superconductor rapid single flux quantum logic device has been also proposed.

[0008] FIG. 2 shows a circuit configuration of a conventional half adder using the superconductor rapid single flux quantum logic device as a logic circuit. The half adder is rapidly operated at an operating speed of approximately several tens GHz. In FIG. 2, circuit components denoted by J represent Josephson junctions.

[0009] Josephson junction is obtained by weakly combining two superconductors with each other. When an input signal is applied to the Josephson junction, a current of more than a predetermined level is flowed through the Josephson junction to generate a very short voltage pulse of several ps. Accordingly, a digital logic gate having a high operating speed of several tens to hundreds GHz can be constructed using the Josephson junction.

[00010] In addition to the aforementioned half adder, a T flip-flop using the superconductor rapid single flux quantum logic device as a logic circuit has been proposed. This T flip-flop is operated very rapidly at an operation speed of 770GHz.

[00011] Recently, there are attempts to utilize the half adder using the superconductor rapid single flux quantum logic device as a logic circuit for ALUs.

Summary Of The Invention

[00012] Accordingly, the present invention has been made in view of the aforementioned technical trends, and it is an object of the present invention is to provide a high-performance ALU that can be operated as an OR gate, an AND gate, an adder gate and an exclusive OR gate using a half adder that uses a superconductor rapid single flux quantum logic device as a logic circuit.

[00013] To accomplish the above object, according to the present invention, there is provided an ALU using a half adder comprising a half adder using a superconductor rapid single flux quantum logic device as a logic circuit, and a switching unit that has input ports respectively connected to a sum output port and a carry output port of the half adder and is operated as an OR gate, an AND gate, an adder gate and an exclusive OR gate using output signals of the half adder. The switching unit includes a first switch having an input port connected to the sum output port of the half adder, a second switch having an input port connected to the carry output port of the half adder and an output port connected to an output port of the first switch, and a third switch having an input port connected to the carry output port of the half adder.

Brief Description Of Drawings

[00014] The above and other objects, features and advantages of the present invention will be apparent from the following detailed description of the preferred embodiments of the invention in conjunction with the accompanying drawings, in which:

[00015] FIG. 1 shows a structure of an ALU generally used;

[00016] FIG. 2 shows a circuit configuration of a half adder using a superconductor rapid single flux quantum logic device as a logic circuit;

[00017] FIG. 3 shows a configuration of an ALU using a half adder according to an embodiment of the present invention;

[00018] FIG. 4 shows a configuration of a switch of the ALU of FIG. 3;

[00019] FIG. 5 shows a configuration of a 2-bit ALU employing the ALU using a half adder according to an embodiment of the present invention; and

[00020] FIG. 6 shows a configuration of a 4-bit ALU employing the ALU using a half adder according to an embodiment of the present invention.

Detailed Description Of Preferred Embodiments

[00021] The present invention will now be described more fully with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. The invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. It will be appreciated that various modifications, variations or equivalent arrangements which may occur to those skilled in the art should be considered to be within the scope of the invention.

[00022] FIG. 3 shows a configuration of an ALU using a half adder according to an embodiment of the present invention. Referring to FIG. 3, the ALU includes a half adder 20 that uses a superconductor rapid single flux quantum logic device as a logic circuit, and a switching unit 30 that has input ports respectively connected to a sum output port S and a carry output port C of the half adder 20. The ALU is operated as an OR gate, an AND gate, an adder or an exclusive OR gate using output signals of the half adder 20. The

switching unit 30 includes a first switch 31 having an input port connected to the sum output port S of the half adder 20, a second switch 32 having an input port connected to the carry output port C of the half adder 20 and an output port connected to an output port of the first switch 31, and a third switch 33 having an input port connected to the carry output port C of the half adder 20.

[00023] FIG. 4 shows a configuration of each of the first, second and third switches shown in FIG. 3. In FIG. 4, circuit elements denoted by J represent Josephson junctions.

[00024] The switch shown in FIG. 4 is closed when a current magnitude of a control signal Switch Control is larger than a predetermined value determined by values of the circuit elements. The switch is opened when the current magnitude is less than the predetermined value. When an input signal is applied to the switch through an input inductor, a first Josephson junction Joff does not generate a voltage pulse when the switch is opened and a second Josephson junction Jon generates a voltage pulse when the switch is closed. The voltage pulse is output through an output inductor.

[00025] The operation of the ALU using the half adder according to the present invention will be explained hereinafter.

[00026] The ALU using the half adder 20 shown in FIG. 3 is operated as an OR gate, an AND gate, an adder gate or an exclusive OR gate on the basis of states of the first, second and third switches 31,32 and 33 of the switching unit 30. Specifically, the ALU is operated as an OR gate when the first and second switches 31 and 32 are closed and the third switch 33 is opened. The ALU is operated as an AND gate when the second switch 32 is closed and the first and third switches 31 and 33 are opened. The ALU is operated as an adder gate when the first and third switches 31 and 33 are

closed and the second switch 32 is opened. The ALU is operated as an exclusive OR gate when the first switch 31 is closed and the second and third switches 32 and 33 are opened.

[00027] A 2-bit ALU as shown in FIG. 5 can be constructed using the above-described operation characteristic. FIG. 5 shows a configuration of the 2-bit ALU employing the ALU using a half adder according to the present invention. The 2-bit ALU includes three half adders 41, 42 and 43, two switching units 43 and 44, and two D flip-flops 45 and 47. The operation of the 2-bit ALU will be explained hereinafter in detail.

[00028] In the case where the 2-bit ALU is set to an OR gate, when two 2-bit inputs, for example, 11 (A1=1, A0=1) and 10 (B1=1, B0=0) are applied to input ports of the 2-bit ALU, ORed results are output through output ports R0 and R1 so that an output value 011 (R2=0, R1=1, R0=1) is obtained. In this case, the output port R2 outputs 0 all the time.

[00029] In the case where the 2-bit ALU is set to an AND gate, when two 2-bit inputs, for example, 11 (A1=1, A0=1) and 10 (B1=1, B0=0) are applied to the input ports of the 2-bit ALU, ANDed results are output through the output ports R0 and R1 so that an output value 010 (R2=0, R1=1, R0=0) is obtained. In this case, the output port R2 outputs 0 all the time.

[00030] In the case where the 2-bit ALU is set to an adder gate, when two 2-bit inputs, for example, 11 (A1=1, A0=1) and 10 (B1=1, B0=0) are applied to the input ports of the 2-bit ALU, added results are output through the output ports R0 and R1 so that an output value 101 (R2=1, R1=0, R0=1) is obtained.

[00031] In the case where the 2-bit ALU is set to an exclusive OR gate, when two 2-bit inputs, for example, 11 (A1=1, A0=1) and 10 (B1=1,

B0=0) are applied to the input ports of the 2-bit ALU, exclusive-ORed results are output through the output ports R0 and R1 so that an output value 001 (R2=0, R1=0, R0=1) is obtained. In this case, the output port R2 outputs 0 all the time.

[00032] In the meantime, an ALU that can process multiple bits is required for practical uses.

[00033] FIG. 6 shows a configuration of a 4-bit ALU employing the ALU using a half adder according to the present invention. The 4-bit ALU includes ten half adders 51, 52, 53, 54, 60, 61, 62, 66, 67 and 72, four switching units 55, 56, 57 and 58, fourteen D flip-flops 59, 63, 64, 65, 68, 69, 70, 71 and 73 through 78.

[00034] A maximum operating speed of a circuit that determines a digital value using a voltage pulse is decided according to a signal delay of the voltage pulse. Thus, the operating speed of the circuit is reduced when the circuit uses a global clock used by a circuit that determines a digital value according to a voltage state. Accordingly, the circuit that determines a digital value using a voltage pulse does not require the global pulse.

[00035] That is, the 4-bit ALU shown in FIG. 6 can use a local clock because only component circuits arranged in each row are required to be operated in one clock cycle. Accordingly, a signal delay of the voltage pulse is reduced to increase a maximum operating speed of the circuit. Furthermore, the circuit becomes less sensitive to an increase in the number of bits.

[00036] The operation of the 4-bit ALU shown in FIG. 6 will be explained hereinafter in detail.

[00037] In the case where the 4-bit ALU is set to an OR gate, when two 4-bit inputs, for example, 1111 and 1010 are applied to the circuit, an output value 01111 is obtained.

[00038] In the case where the 4-bit ALU is set to an AND gate, when two 4-bit inputs, for example, 1111 and 1010 are applied to the circuit, an output value 01010 is obtained.

[00039] In the case where the 4-bit ALU is set to an adder gate, when two 4-bit inputs, for example, 1111 and 1010 are applied to the circuit, an output value 11001 is obtained.

[00040] In the case where the 4-bit ALU is set to an exclusive OR gate, when two 4-bit inputs, for example, 1111 and 1010 are applied to the circuit, an output value 00101 is obtained.

[00041] As described above, the present invention can produce a high-performance ALU that can be operated as an OR gate, an AND gate, an adder and an exclusive OR gate using a half adder that uses a superconductor rapid single flux quantum logic device as a logic circuit.

[00042] While the present invention has been described with reference to the particular illustrative embodiments, it is not to be restricted by the embodiments but only by the appended claims. It is to be appreciated that those skilled in the art can change or modify the embodiments without departing from the scope and spirit of the present invention.